MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A
We, INTERNATIONAL STANDARD ELECTRIC CORPORATION of 320 Park Avenue, New York 22, State of New York, United States of America, hereby apply for the grant of a Patent for an invention, entitled, "A COMPUTER MEMORY ACCESS CIRCUIT" which is described in the accompanying complete specification. This application is a Convention application and is based on the application numbered P 27 10 671.4 for a patent or similar protection made in the Federal Republic of Germany on 11 March, 1977.

Our address for service is:

PATENT DEPARTMENT,
STANDARD TELEPHONES AND CABLES PTY. LIMITED,
252-280 BOTANY ROAD,
ALEXANDRIA, N.S.W. 2015.
AUSTRALIA.

Dated this seventh day of March,

INTERNATIONAL STANDARD ELECTRIC CORPORATION

Authorized Signatory

To: The Commissioner of Patents.
FORM 8
COMMONWEALTH OF AUSTRALIA
PATENTS ACT 1952 - 1969

DECLARATION IN SUPPORT OF A CONVENTION APPLICATION FOR A PATENT OR A PATENT OF ADDITION

In support of the convention application made for a patent of addition for an invention entitled

"A COMPUTER MEMORY ACCESS CIRCUIT"

I, CONWAY WALTER WADHAM,
of Standard Telephones and Cables Pty. Limited, 252-280 Botany Road, Alexandria, 2015, N.S.W., Australia, do solemnly and sincerely declare as follows:—

1. I am authorised by INTERNATIONAL STANDARD ELECTRIC CORPORATION the applicant for the patent of addition to make this declaration on its behalf
2. The basic application as defined by Section 141 of the Act was made in the Federal Republic of Germany on 11 March, 1977 by STANDARD ELEKTRIK LORENZ AKTIENGESELLSCHAFT.
3. DIETRICH ILLI of Max-Brod-Weg 14, 7000 Stuttgart 40, Germany, HERMANN-JOSEF GOLBACH of Neuffenstrasse 38, 7141 Mößingen, Germany and CLAUSJÜRGEN BECHERER of Zellerstrasse 69, 7000 Stuttgart 1, Germany are the actual inventors of the invention, and the facts upon which the Applicant is entitled to make the application are as follows:—

INTERNATIONAL STANDARD ELECTRIC CORPORATION is the Assignee of STANDARD ELEKTRIK LORENZ AKTIENGESELLSCHAFT who are the Assignees of THE SAID INVENTORS.

4. The basic application referred to in paragraph 2 of this Declaration was made the first application in a Convention country in respect of the invention the subject of the application.

Declared at SYDNEY this 7th day of March, 1978.

INTERNATIONAL STANDARD ELECTRIC CORPORATION

To: The Commissioner of Patents

[Signature]
1. A data memory access circuit to connect a program memory and a data memory of a processor comprising an instruction decoder to decode instructions from the program memory, first switching means controlled by the decoder to switch a direct address in an instruction to the data memory address input or to switch a base address to a base memory and to switch a relative address to an adder, the base memory output also being connected to the adder, the adder output being connected to data memory address input.

5. A computer controlled telecommunication switching system including a circuit as claimed in any one of the preceding claims.
COMMONWEALTH OF AUSTRALIA
PATENTS ACT 1952-1969

COMPLETE SPECIFICATION FOR THE INVENTION ENTITLED

"A COMPUTER MEMORY ACCESS CIRCUIT"

The following statement is a full description of this invention, including the best method of performing it known to us:-
The present invention relates to a circuit arrangement for controlling access to the data memory of a microprocessor co-operating with a program memory, for example, for computer-controlled telecommunication switching systems.

If a great measure of flexibility is required in controlling data memory access, the microprocessor must be capable of using indirect addressing. To do this, it is common practice to fetch a macroinstruction by accessing the program memory. The microprocessor receives this macroinstruction and addresses the data memory with the address contained in this instruction. The data memory access yields a base address which the microprocessor adds to the relative address stored in it and contained in the operation code of the macroinstruction. The sum is the effective address which can be used to access the data memory in the next microprocessor cycle. After instruction decoding, the microprocessor must perform several microcycles to obtain the desired data. Since the number of cycles to be performed is a factor determining the time required for processing, the data flow rate is correspondingly lower than with direct addressing. Still, for programming reasons, real-time systems with many users cannot do without indirect addressing.

This system may be used to address, for example, a table of data such that the base address locates the table and the relative address defines the particular location of the data in the table. In this invention this process is performed in external circuitry, saving processor time.

The object of the invention is to provide a circuit arrangement for controlling data-memory access. There is described a system in which the instruction output of the program memory and the address input of the data memory are connected to a switching
logic containing an instruction decoder and a switching facility controlled by
the instruction decoder, which, upon receipt of a macroinstruction with a
direct address in its address part, influences the switching facility via a
control line in such a manner that the direct address is transferred to the
address input of the data memory, that the switching logic is connected to a
separate base memory and to an adding stage outside the microprocessor, that the
instruction decoder, upon receipt of a macroinstruction with a relative
address and a base-memory address in the address part, influences
the switching facility in such a manner that the relative address
is placed in the adding stage, and the base-memory address in the
base memory, that the base memory is connected to the adding
stage, which receives the fetched base address and adds it to the
relative address, and that the adding stage has its sum output
connected to the address input of the data memory. With the cir-
cuit arrangement according to the invention, direct and base-
relative addresses for accessing a data memory can be obtained
during one cycle in any sequence. When base-relative addressing
is used, access time can be reduced to a minimum.

In a further development of the circuit arrangement embodying
the invention, the base memory is a small, fast-access memory.
This permits an address to be obtained within one cycle even if
base-relative addressing is used.

An embodiment of the invention will now be described in more
detail with reference to the accompanying drawing. The drawing is
a block diagram of a circuit arrangement for controlling data-
memory access.

It is assumed that the program memory PS delivers a 36-bit-
wide macroinstruction Mb to a switching logic SL. The switching
logic SL includes an instruction decoder BD which decodes the
instruction code contained in the macroinstruction Mb. A result
of the decoding can indicate that the addressing for the next data-memory access is to be (a) direct or (b) base-relative. Other possible addressing modes, which do not form part of the invention, will not be described here.

In case (a), the address A contained in the macroinstruction Mb - a direct address dA, is transferred as an effective address eA to the address input AE of the data memory DS via switching facilities SE1 and SE2 controlled by the instruction decoder BD. The switching facilities SE1, 2 contain multiplexers which switch the address A through in response to the control instruction coming from the instruction decoder BD via a control line S.

In case (b), the program memory PS delivers a macroinstruction Mb which consists of an instruction code and of a relative address rA (cf. introductory remarks) and a base-memory bsA in the address part. The base-memory address bsA is fed via the multiplexer in the switching facility SE1 to a small and fast base memory BS containing in the base address bd, which is fetched and fed to the adder Add where it is added to the relative address rA. The sum so obtained is the effective address for the desired data-memory access; it is transferred as an effective address eA to the address input AE of the data memory DS via the multiplexer SE2 under the control of the instruction decoder BD.

The base-relative addressing described is especially suited for use in real-time systems in which many users operate with a common program, e.g. in computer-controlled switching systems. In that case, base-relative addressing is used to address problem-dependent variable data. The address of a data structure is considered the base address bd; a plurality of data structures may be allotted to each problem to be handled in a computer. The relative address rA specifies a given location within the base
addressed and problem-oriented data structure.
The claims defining the invention are as follows:
1. A data memory access circuit to connect a program memory and a data memory of a processor comprising an instruction decoder to decode instructions from the program memory, first switching means controlled by the decoder to switch a direct address in an instruction to the data memory address input or to switch a base address to a base memory and to switch a relative address to an adder, the base memory output also being connected to the adder, the adder output being connected to data memory address input.
2. A circuit as claimed in claim 1 in which the direct address and the adder output are connected to the data memory address input via second switching means controlled by the instruction decoder.
3. A circuit as claimed in claim 1 or claim 2 in which the base memory is a fast access memory.
4. A data memory access circuit substantially as herein described with reference to the accompanying drawing.
5. A computer controlled telecommunication switching system including a circuit as claimed in any one of the preceding claims.

DATED THIS SIXTH DAY OF MARCH, 1978.

INTERNATIONAL STANDARD ELECTRIC CORPORATION