Application for a Standard Patent or
A Standard Patent of Addition

We, INTERNATIONAL STANDARD ELECTRIC CORPORATION
of 320 Park Avenue, New York 22, State of New York, United States of
America, hereby apply for the grant of a standard patent
for an invention, entitled

"AN ELECTRONIC GATING ARRANGEMENT"

which is described in the accompanying complete specification.
Details of basic application(s) -
Number of basic application 2/60206
Name of Convention country in which basic application was filed: Belgium
Date of basic application 19 September 1983

Our address for service is:

PATENT DEPARTMENT,
STANDARD TELEPHONES AND CABLES PTY. LIMITED,
252-280 BOTANY ROAD,
ALEXANDRIA, N.S.W. 2015.
AUSTRALIA,

Dated this Eleventh day of September 1984

INTERNATIONAL STANDARD ELECTRIC CORPORATION

Authorized Signatory

To: The Commissioner of Patents

The present invention relates to gating means.
A known gating means is for instance a transistor switch, which may be
used for interconnecting two points belonging to respective circuits. However,
FORM 8
COMMONWEALTH OF AUSTRALIA
PATENTS ACT 1952-1969

DECLARATION IN SUPPORT OF A CONVENTION
APPLICATION FOR A PATENT OR
A PATENT OF ADDITION

In support of the convention application made for a patent or an addition for an invention entitled
"AN ELECTRONIC GATING ARRANGEMENT"

I, PATRICK MICHAEL CONRICK,
of Standard Telephones and Cables Pty. Limited, 252-280 Botany Road, Alexandria, 2015, N.S.W. Australia, do solemnly and sincerely declare as follows:–

1. I am authorised by INTERNATIONAL STANDARD ELECTRIC CORPORATION
the applicant for the patent or addition to make this declaration on its behalf
2. The basic application as defined by Section 141 of the Act was
made in Belgium
on 19 September, 1983
by BELL TELEPHONE MANUFACTURING COMPANY, NV
3. DANIEL SALABRITS, of Kouterstraat 19, B-3220
AARSCHOT, Belgium
and
MICHEL, CAMILLE AUGUSTE RENE RABIEN, of
Termikkelaan 16, B-2530 BOECHOUT, Belgium,

are the actual inventors of the invention, and the facts upon which the Applicant
is entitled to make the application are as follows:

INTERNATIONAL STANDARD ELECTRIC CORPORATION is the Assignee of
BELL TELEPHONE MANUFACTURING COMPANY, NV, is the Assignee
of the Said Inventors.

4. The basic application referred to in paragraph 2 of this Declaration was
the first application in a Convention country in respect of the invention the subject
of the application.

Declared at Sydney this 11th day of September 1984
INTERNATIONAL STANDARD ELECTRIC CORPORATION

To: The Commissioner of Patents
Declarant
An electronic gating arrangement comprising: a first inverter to the input of which first and second switches are connected, the first switch being controllable by a first switching signal to connect a first input signal to the first inverter's input, the second switch being controllable by a second switching signal to connect a reference voltage to the first inverter's input; a second inverter to the input of which third and fourth switches are connected, the third switch being controllable by a third switching signal to connect a second input signal to the second inverter's input, the fourth switch being controllable by a fourth switching signal to connect a reference voltage to the second inverter's input; a fifth switch controllable by the second switching signal to connect the output of the first inverter to the output of the second inverter; a sixth switch controllable by the fourth switching signal to connect the second inverter's output to the first inverter's output.

A test arrangement for testing a plurality of circuits, and including a shift register with a data input and a plurality of cascaded stages each one coupled to the input of a corresponding one of said circuits to be tested an output of which is coupled back to said one stage, wherein each of the stages and the circuits to be tested intercoupled therewith constitute a gating means as claimed in any one of claims 1 to 12, said first and second inverters being included in the stage and in the circuit to be tested respectively.
The following statement is a full description of this invention, including the best method of performing it known to us:—
The present invention relates to gating means. A known gating means is for instance a transistor switch, which may be used for interconnecting two points belonging to respective circuits. However, such a gating means is not able to transform a logic state in one point to a logical state in the other point and vice-versa.

It is desirable to provide a gating means of the above type, but additionally able to selectively transfer logical states between the circuits.

The specification describes a gating means which includes first and second logic means each able to assume at least two distinct input logic states and at least two distinct output logical states and controlled means to intercouple the logical means so that upon the logical means being intercoupled and one logical means assuming a predetermined input logical state its output logical state becomes a predetermined function of the output logical state of the other logical means.

In a modification of the gating means each of the logical means has an output able to assume the logical output state, and that the controlled intercoupling means are able to intercouple the output of the two logical means.

In a further option each of the logical means is able to assume at least the predetermined or first input state wherein a first and a second voltage are connected to the output via a lower and a higher impedance respectively, the output then assuming a first output state, and able to assume a second input state wherein the first and second voltages are connected to the output via a lower and a higher impedance respectively, the output then assuming a second output state.

Thus current is able to flow between the two logical means and to modify the voltage at the output of the one logical means assuming the predetermined state to a voltage which is function of the state of the output of the other logical means.

The present gating means thus permits e.g. the transfer of data between two points in a very simple way.

There is also described a test arrangement for testing a plurality of circuits, and including a shift register with a data input and plurality of cascaded stages each one coupled to the input of a corresponding one of the circuits to be tested an output of which is coupled back to the one stage.


In this known test arrangement, as shown in Fig. 4 of the article, each
shift register stage comprises two series connected first and second latch circuits the junction point of which is directly connected to the input of the associated circuit to be tested, the latter circuit having an output which is directly connected back to the first latch circuit. The first latch circuits are controlled by shift pulses A and C1 (system clock) whilst the second latch circuits are controlled by shift pulses B. To check the operation of the circuits to be tested first an input test pattern of binary states is stored in the shift register with the help of the shift pulses A and B so that a predetermined binary state is thus applied to the input of each circuit to be tested. These circuits then perform a test operation and when the latter is finished a test output pattern appears at the outputs thereof. The latter pattern is then registered in the shift register stages by means of the shift pulses C1 and B and by overwriting the data previously stored therein. Afterwards the test output pattern is shifted out with the help of the shift pulses A and B and compared with the test input pattern to evaluate the condition of the circuits which have been tested.

In this known test arrangement, during the time when the circuits under test perform their operation the test input pattern applied to their inputs should not be altered by an external cause, e.g. by shifting the shift register contents, in order not to influence the operation of the circuits under test. As a consequence during such an operation the shift register cannot be used for other purposes.

It is desirable to provide a test arrangement of the above type but which does not present this drawback. This may be achieved due to the fact that each of the stages and the circuit to be tested intercoupled together constitute a gating means as described above, the first and second logical means being included in the stage and in the circuit to be tested respectively.

The controlled intercoupling means included in the gating means enable the shift register to be connected to or disconnected from the circuits to be tested. As such a connection is only established during the time intervals when the input test pattern is applied from the shift register to the circuits to be tested and when the output test pattern is applied from the latter circuits to the shift register, the free use of the shift register is permitted except during the time data is transferred between the shift register and the circuits to be tested.

Another advantage of the present test arrangement is that this transfer is performed in a simple way by the gating means, as already mentioned above.

The abovementioned and other objects and features of the invention will
The first gating circuit SGC1 includes two logical means or inverters SINV11 and SINV12 and five gating means constituted by NMOS transistors ST11 to ST15, whilst the second gating circuit TGC1 includes two inverters TINV11 and TINV12 and five gating means constituted by NMOS transistors TT11 to TT15.

In the inverter SINV11 the NMOS depletion transistor ST11 constitutes a load for enhancement transistor ST12 as its drain electrode is connected to the positive voltage V+ and its source to the drain electrode of ST12 whose source electrode is connected to ground. The gate and source electrodes G and S of ST11 and the drain electrode D of ST12 are all connected to the input terminal S11 via the series connection of transistor ST13 controlled by the control pulses A and to ground via transistor ST14 controlled by the control pulses R. The inverter output S011 is connected to the output terminal SO1 via the series connection of transistor ST15 controlled by the control pulses B and the inverter SINV12 which is identical to SINV11.

The various components of the second gating circuit TGC1 are connected in a similar way as those of the first gating circuit SGC1, but with a phase shift between the control pulses A, B, R and W, which is more apparent and the inversion itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings therein.

**Fig. 1** shows a test arrangement using the gating means of Fig. 1.

**Fig. 2** represents control pulses used in the gating means according to Fig. 1.

**Fig. 3** shows a test arrangement using the gating means of Fig. 1.

The first gating circuit SGC1 has a data input S11, a data output SO1 and three control inputs A, B and R, whilst the second gating circuit TGC1 has a data input T11, a data output TO1 and three control inputs A, B and W. The control signals A, B, R and W are applied from a control signal source (not shown). From this figure it is seen that the control pulses A and B are in phase opposition, whilst the control pulses R and W, when occurring, each overlap a pair of consecutive A and B pulses. From this figure it is seen that the control pulses A and B are in phase opposition, whilst the control pulses R and W, when occurring, each overlap a pair of consecutive A and B pulses.
TT14 is controlled by the control pulses W.

The controlled intercoupling means IM1 includes transistors ST16 and TT16 which are each connected between the outputs or nodes S011 and T011 of SGC1 and TGC1 and which are controlled by the control pulses R and W respectively.

The above inverters each have two stable operating states:
- a first one which occurs when the gate/source voltage of ST12 is 0 Volt (binary 0). In this case the drain/source voltages of ST11 and ST12 are equal to 0 Volt and 5 Volts respectively, ST11 being conductive and ST12 being blocked. A binary 1 then appears at output S011;
- a second state which occurs when the gate/source voltage of ST12 is 5 Volts (binary 1). In this case the drain/source voltage of ST11 is about 5 Volts and ST12 0 Volts, ST11 being then blocked and ST12 conductive. A binary 0 then appears at output S011.

Hence, inverter SINV11 is a logical means able to assume two distinct input logic states and two distinct output logical states and depending on the binary value applied at its input SINV11 being 0 (ground) or 1 (+V) this logical means is:
- in a first input state wherein ST11 is conductive and ST12 is blocked, the first output state being then 1 since a 1 then appears at the output S011. In this state ST11 and ST12 constitute a higher and a lower impedance respectively;
- in a second input state wherein ST12 is conductive and ST11 is blocked, the second output state being then 0 since a 0 then appears at the output S011. In this state ST11 and ST12 constitute a lower and a higher impedance respectively.

Also the inverters SINV12, TINV11 and TINV12 which are similar to SINV11 can assume two distinct input states and two distinct output states.

The above described bidirectional gating means permits the transfer of binary data from either one of the input terminals SIl and TIl to either one of the output terminals S01 and T01 as it enables the bidirectional transfer of binary data between the outputs S011 and T011 via the intercoupling means IM1.

First the transfer from SIl to TIl is considered. When a binary value 0 (ground) or 1 (+V) is present at the input terminal SIl, it is transferred to the output terminal S01 by means of two successive control pulses A and B, such as A,1 and B,1 of Fig. 2. Control pulse A,1 makes transistor ST13 conductive and thus transfers the binary value at SIl to the input SINV11 of SINV11 wherein ST11 or ST12 becomes conductive depending on this binary value being 0 or 1 respectively. As a consequence the binary value 1 (+V)
or 0 (ground) appears at the output SO1. Control pulse B,1 afterwards makes transistor ST15 conductive so as to transfer the binary value at node SO1 to SIN12 and then after inversion from SIN12 to SO1 so that the same binary value as at SI1 appears at SO1.

In a like way binary data may be transferred from T1 to TO1.

The transfer of binary data from input terminal SI1 to output terminal TO1 is now considered, it being supposed that arbitrary binary values are present at the input terminals SI1 and TI1, as well as at the output terminals SO1 and TO1. This transfer is performed for instance under the control of the two consecutive control pulses A,2 and B,2 and of the control pulse W which overlaps A,2 and B,2 as shown in Fig. 2.

By the control pulses A,2 and W the transistors ST13, TT13 and TT14, TT16 are rendered conductive. As a consequence SI1 is connected to the input SIN11 of inverter SINV11 the output SO11 of which is connected to the output TO11 of inverter TINV11, and ground is connected to input TIN11 of the latter inverter TINV11. As a result the binary value at SI1 appears in inverted form at node SO11, ST11 or ST12 being conductive depending on this binary value being 0 or 1 respectively. The binary value applied via TT13 to TINV11 has no influence, but the value 0 applied via TT14 makes TT11 conductive due to which +V is connected to TO11 via a lower impedance. As a consequence TO11 becomes 1 when SO11 is on 1 too (ST11 conductive) and is changed to 0 otherwise (ST12 conductive). Indeed, when ST11, TT11 and TT14 are conductive the lower impedances of ST11 and TT11 are branched in parallel via TT16 so that the voltage at TO11 is not changed. On the contrary, when ST11 is blocked and both TT11 and TT14 are conductive the lower impedance of TT11 is branched in parallel with the higher impedance of ST11 via TT16 so that the voltage TO11 is changed to about 0 Volt.

Summarizing, under the control of the control pulses A,2 and W the binary value at the input SI1 appears in inverted form at the node TO11 and the entry of binary data at the input TI1 is blocked.

By the control pulse B,2 the binary value at SO11, TO11 is then transferred from SO11 to SO1 and from TO11 to TO1.

The transfer of binary data from input terminal TI1 to output terminal SO1 is performed, in a similar way as described above, under the control of e.g. the two consecutive control pulses A,m and B,m and of the control pulse R which overlaps A2,m and B2,m as shown in Fig. 2.

From the above it follows that the gating means shown permits a bi-directional transfer of binary data between nodes SO11 and TO11 which the control pulses A and B need not be interrupted during such a transfer under the control of the pulses W or R as their effect is inhibited by ST14.
or TT14 which are anyhow needed to bring S011 or TO11 to a predetermined state which is the 1-state. Each of ST14 and TT14 thus has a double function.

In the above, when one of the logical means SINV11 and TINV11 is in the predetermined input logical state wherein in ST11 or TT11 is conductive and the intercoupling means ST16 or TT16, is made conductive, the output logical state of this one logical means SINV11 or TINV11 becomes equal to the output logical state of the other logical means TINV11 or SINV11 respectively.

Instead of simply allowing a copying of data between S011 and T011 the intercoupling means could also be made to perform any other transformation of the binary data transferred between these nodes.

Referring to Fig. 3 the test arrangement shown therein includes a shift register SR and circuitry to be tested CT, this register SR and circuitry CT being intercoupled by a controlled intercoupling arrangement IA.

Shift register SR has n identical stages S1 to Sn which are connected in cascade and each comprise the series connection of a main shifting stage circuit SMS1 to SMSn and an auxiliary shifting stage circuit SAS1 to SASn controlled by the above control pulses A, R and B respectively. The nodes or junction points S011 and S0n1 of the main and auxiliary circuits in the stages S1 to Sn are connected to the nodes T011 and TOn1 or corresponding circuits to be tested CT1 to CTn respectively via identical controlled intercoupling means IM1 to IMn forming part of the controlled intercoupling arrangement IA. The circuits CT1 to CTn are controlled by the pulses A, B and W, whilst IM1 to IMn are each controlled by the pulses R and W.

Each of the identical shifting stages S1 to Sn is of the same type as the first gating circuit SGC1 described above in relation to Fig. 1.
More particularly, the main and auxiliary shifting stage circuits SMS1 and SAS1 of S1 comprise the components ST11 to ST14 and ST15, SINV12 of Fig. 1 respectively.

Each of the identical controlled intercoupling means IM1 to IMn is of the same structure as the intercoupling means described above in relation to Fig. 1. More particularly, the intercoupling means IM1 includes the components ST16, TT16 shown in Fig. 1.

Each of the circuits to be tested CT1 to CTn for instance includes a structure of the same type as the second gating circuit TGCl described above in relation to Fig. 1 and other circuitry to be tested. More particularly the circuit to be tested. More particularly, the circuit to be tested CT1 includes the second gating circuit TGCl which is included in a loop with other circuitry to be tested such as OCT1, shown in dotted lines in Fig. 1.

In order to simultaneously test the circuits CT1 to CTn an n-bit input test pattern is applied to the general input SI of the shift register SR.
and shifted therethrough by means of the control or shift pulses A and B until the binary values of the input test pattern appear at the inputs S11 to S1n of the stages S1 to Sn. By means of a pair of control or shift pulses A and B and an overlapping control or write pulse W, such as A1, B1 and W1 of Fig. 2, the input test pattern is first applied (by A1 and W) from the inputs of the stages S1 to Sn to the nodes T011 to T0n1 of the circuits CT1 to CTn and then shifted (by B1) to the outputs S01 of the stages S1 to Sn. Thus the input test pattern is entered in the circuits to be tested CT1 to CTn.

After the circuits to be tested have performed their test operation in response to the binary values applied to their inputs a test output pattern appears at the input terminals of these circuits, such as at T011 of CT1. By means of a pair of control or shift pulses A and B and an overlapping control or read pulse R, such as A1, B1 and R, the output test pattern is first applied (by A1 and R) from the inputs of the circuits to be tested T01 to T0n to the nodes T011 to T0n1 of these circuits and to the nodes S01 to T011 of the stages. Afterwards it is shifted (by B1) to the outputs of the stages S1 to Sn. By a series of pulses A and B the test output pattern is then shifted out of the shift register SR and compared with the initial test input pattern to evaluate the condition of the circuits CT1 to CTn.

Due to the presence of the intercoupling means ST16, TT16 which are only operated during a data transfer between the nodes S011 and T011, the shift register SR may be freely used during the time the circuits to be tested CT1 to CTn perform their test operation, without affecting this operation. For instance, the shift register SR could be associated to a plurality of sets of circuits to be tested and, during the time of a test operation is being performed in one set, could be transferred between the shift register and the circuits of another set. Another example is that wherein two shift registers are associated to a set of circuits to be tested. In this case one shift register may for instance be used to transmit input data to the set and the other to receive output data from the set. During each such transfer from or to one shift register new data can be entered in or shifted out of the other shift register.

To be noted that instead of the inverters other logical means having a same output circuit as these inverters could be used.
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The claims defining the invention are as follows:

1. An electronic gating arrangement comprising: a first inverter to the input of which first and second switches are connected, the first switch being controllable by a first switching signal to connect a first input signal to the first inverter's input, the second switch being controllable by a second switching signal to connect a reference voltage to the first inverter's input; a second inverter to the input of which third and fourth switches are connected, the third switch being controllable by a third switching signal to connect a second input signal to the second inverter's input, the fourth switch being controllable by a fourth switching signal to connect a reference voltage to the second inverter's input; a fifth switch controllable by the second switching signal to connect the output of the first inverter to the output of the second inverter; a sixth switch controllable by the fourth switching signal to connect the second inverter's output to the first inverter's output.

2. A gating arrangement as claimed in claim 1, wherein the third switching signal is the same as the first switching signal, and the fourth switching signal is the inverse of the second switching signal.

3. A gating arrangement as claimed in claim 1 or 2 wherein the output of the first inverter is connected to the input of a third inverter via a seventh switch controlled by a seventh switching signal, and wherein the output of the second inverter is connected to the input of a fourth inverter by an eighth switch controlled by an eighth switching signal.

4. A gating arrangement as claimed in claim 3 wherein the eighth switching signal is the same as the seventh switching signal.

5. A gating arrangement as claimed in any one of claims 1 to 4 wherein each inverter comprises a first and second transistor with their main current paths connected in series between a voltage source and the reference voltage, the control electrode of the first transistor being connected to the junction of the first and second transistors main current paths, the control electrode of the second transistor being the inverter input, the said junction being the inverter output.

6. A gating arrangement as claimed in claim 5, wherein the first transistor has its main current path opposite said junction connected to the voltage source and the second transistor has its main current path opposite said junction connected to the reference voltage.

7. A gating arrangement as claimed in claim 1 or any other claim appending thereto wherein an operating pulse of the second signal overlaps a first mark-space period of a first switching signal pulse, and wherein an operating pulse of the fourth switching signal overlaps a second mark-space period of...
a further first switching signal pulse.

8. An electronic gating arrangement including first and second logical means each able to assume at least two distinct input logical states and at least two distinct output logical states and controlled means to intercouple the logical means so that upon the logical means being intercoupled and one logical means assuming a predetermined input logical state its output logical state becomes a predetermined function of the output logical state of the other logical means.

9. A gating arrangement according to claim 8, wherein the input of each of the logical means is coupled via a first gating means to a source of input signals having said first or second condition, the first gating means being controlled by a first control signal source generating first control signals and wherein the input of each of the logical means is coupled via a second gating means to a reference voltage having the first condition, the second gating means coupled to the input of the first and second logical means being able to be controlled by second and fourth control signals respectively, the controlled intercoupling means being constituted by a third gating means controlled by the second and fourth control signals.

10. A gating arrangement as claimed in claim 5 or any claim appended thereto wherein the first transistors are depletion field effect transistors and the second transistors are enhancement field effect transistors of the same polarity and each having source, drain and gate electrodes, the drain and source electrodes of said transistors being connected in series between the voltage source and the reference voltage, the gate electrode of the enhancement transistor constituting the output and the gate and source electrodes of the depletion transistor being interconnected and constituting the output.

11. A gating arrangement according to claim 10, wherein the depletion and enhancement transistors are of the n-type.

12. An electronic gating arrangement as herein described with reference to the accompanying drawings.

13. A test arrangement for testing a plurality of circuits, and including a shift register with a data input and a plurality of cascaded stages each one coupled to the input of a corresponding one of said circuits to be tested an output of which is coupled back to said one stage, wherein each of the stages and the circuits to be tested intercoupled therewith together constitute a gating means as claimed in any one of claims 1 to 12, said first and second inverters being included in the stage and in the circuit to be tested respectively.
14. An electronic circuit testing arrangement for testing one or more circuits, the testing arrangement comprising an electronic gating arrangement as claimed in any one of claims 1 to 12 and wherein the input of the circuit under test is connected to the output of the second inverter via a switchable further inverter, the output of the circuit under test being connected to the input to the second inverter.

15. An electronic circuit testing arrangement as herein described with reference to the accompanying drawings.

DATED THIS ELEVENTH DAY OF SEPTEMBER 1984

INTERNATIONAL STANDARD ELECTRIC CORPORATION
In this known test arrangement, as shown in Fig. 4 of the article, each
FIG. 2

FIG. 3