PATENT APPLICATION FORM (CONVENTION AND NON-CONVENTION)
COMMONWEALTH OF AUSTRALIA
Regulation 9
Patents Act 1952

APPLICATION FOR A STANDARD PATENT OR
A STANDARD PATENT OF ADDITION

DEERE & COMPANY

John Deere Road, Moline, Illinois 61265 U.S.A.

hereby apply for the grant of a (a) Standard Patent, for an invention entitled (b) NON-VOLATILE MEMORY FAILURE DETECT

which is described in the accompanying (c) complete specification.

For a Convention application — details of basic application(s)

<table>
<thead>
<tr>
<th>NUMBER</th>
<th>COUNTRY</th>
<th>DATE OF APPLICATION</th>
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<td>470,040</td>
<td>U.S.A.</td>
<td>28 February 1983</td>
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We request that the Patent be granted as a Patent of Addition.

My/Our address for service is ARTHUR S. CAVE & CO., Patent and Trade Mark Attorneys, 1 Alfred Street, Sydney, New South Wales, Australia 2000.

Commissioner of Patents
ARTHRUS, CAVE & CO.
PATENT AND TRADE MARK ATTORNEYS
SYDNEY

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24 FEB 1984

By their Patent Attorneys
ARTHRUS, CAVE & CO.

JAMES G. SIELY P.I.P.A.A.

Background of the Invention

The present invention relates to a control system with a battery power.
1. In a control system having parameter sensing means, first storage means for storing a first data set, including a flag value, second storage means for storing a second data set and a stored program digital computer for generating control signals as a function of variables derived from the sensed parameters and the data sets by execution of a control algorithm, a memory failure detection system comprising:

- means for examining the status of the flag value stored in the first storage means;
- means for setting selected ones of the variables to values corresponding to the second data set prior to execution of the control algorithm when the flag value is in a first state, and for preventing setting of the selected variables to values corresponding to the second data set when the flag value is in a second state; and
- means for setting the flag value to its second state after the selected variables are set to the values corresponding to the second data set.
TO BE COMPLETED BY APPLICANT

Name of Applicant: DEERE & COMPANY

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Complete Specification for the invention entitled:
NON-VOLATILE MEMORY FAILURE DETECT

The following statement is a full description of this invention, including the best method of performing it known to me:-
NON-VOLATILE MEMORY FAILURE DETECT

Background of the Invention

The present invention relates to a control system with a stored program digital computer and a memory associated therewith.

It is known to provide a vehicle with a stored program digital computer or a microprocessor-implemented control system, such as the hitch control system described in U.S. Patent No. 4,013,875. Such a microprocessor-based system may include a programmable read only memory (PROM) for storing factory programmed, non-changing values and random access (read-write) memory (RAM) for storing working values which are recalculated during operation of the system. In certain cases, it may be desirable to initialize certain of these working values to values stored in PROM only upon initial start-up of the control system, and thereafter utilize values stored in RAM.

However, most RAMs are volatile and are cleared upon loss of power. Furthermore, in a sensor-based control system, there may be certain values, such as sensor calibration values, which require more permanent storage, but which must be updated during operation in the field. This suggests that such values be stored in non-volatile RAMs which retain their data even upon loss of power. However, even non-volatile RAMs can fail after extended use. Therefore, it would be desirable to have a control system which is capable of detecting such failures and responding in an appropriate manner.

Summary of the Invention

An object of the present invention is to provide a microprocessor-based control system with a memory failure detecting capability.

It is a further object of this invention to provide such a control system with the capability of utilizing data stored in one memory during normal operation and using data stored in another memory upon initial start-up and during subsequent start-ups upon failure of the one memory.

These and other objects are achieved by the present invention which includes a microprocessor coupled via a data bus to a programmable read only memory (PROM), to a random access memory (RAM), and to other input/output devices. The RAM
is preferably made non-volatile by reason of its dedicated battery power supply. The microprocessor is programmed to set certain variables used in a main control algorithm to values stored in the PROM only upon initial start-up of the control system or upon subsequent start-up if there has been a failure of the RAM.

**Brief Description of the Drawings**

Fig. 1 is a simplified block diagram of the components of the present invention; and

Fig. 2 is a flow chart of the routine performed by the microprocessor of the present invention.

**Detailed Description**

A microprocessor-base control system 10 includes a microprocessor 12 which is coupled via data bus 14 to a random access memory (RAM) 16 and to a programmable read-only memory (PROM) 18. Preferably, the RAM is non-volatile by reason of its dedicated power supply provided by battery 20. The data bus 14 is also coupled to the appropriate input and output devices such as conventional A/D and D/A converters (not shown), multiplexers (not shown), control system input parameter sensors 23, and controlled function actuators 25. These devices may be varied, depending upon the system which is to be controlled, and form no part of the present invention. U. S. Patent Application, Serial No. 360,748, filed 22 March 1982, illustrates one possible arrangement in the context of a vehicle-hitch operation control system and is herein incorporated by reference.

The PROM 18 stores certain values, such as default initialization values, the use of which will be explained later. The non-volatile RAM 16 stores various values which are calculated and used during operation of a control algorithm. The particular control algorithm forms no part of the present invention, but it suffices to mention that the particular values stored in RAM 16 would vary, depending upon the particular control algorithm which is used. An example of such a control algorithm may be found in the aforementioned U. S. Application, Ser. No. 360,748. In addition, a memory status or flag value, for example, BATTERY = 10101010, is also stored in the RAM 16 for use in the memory failure detect procedure described below.
This invention is implemented by executing the procedure illustrated by the flow chart shown in Fig. 2, which starts at step 90. Then, in step 92, the BATTERY value in RAM 16 is compared to a chosen value, for example, the binary number 10101010. Prior to the initial execution of step 92, the BATTERY value may be established at some value other than binary 10101010, so that step 92 initially directs the algorithm to step 94.

In step 94, various values, such as control set point or reference values, or filtered sensor input values, may be initialized to desired preset initial values. Then, in step 96, the BATTERY value is set equal to 10101010, so that the next time through the routine, step 92 will direct the routine directly to step 100 where the main control loop begins. In any case, step 100 may be entered following step 96, whereafter, in step 102, the values the input parameter sensors (not shown) may be read. Then, the main control algorithm 300 may be executed. Again, as previously mentioned, the particular control algorithm forms no part of the present invention and would vary, depending upon the particular functions being controlled. It should suffice here to mention that the control algorithm generates control signals as a function of various set point and sensed input values. These control signals would be communicated via data bus 14 to appropriate function actuators (not shown). Upon execution of the main control algorithm 300, the loop returns to loop start step 100, whereupon the sensed input values are updated in step 102 before the main control algorithm 300 is repeated. This loop involving steps 100, 102 and main control algorithm is repeated until the control system is turned off.

When the control system is restarted, step 90 is entered and then step 92 examines the BATTERY value. If the RAM 16 has not failed, then the routine will be directed to step 100 and the main control algorithm 300 will be executed utilizing the set point and reference values established and stored in the RAM 16 during previous operation of the control system. In this case, the control system can, upon restarting, immediately begin operating using the previously determined set point and reference values, without having those values redetermined.
from the initialization values stored in PROM 18 by repeated interactions of steps 100, 102 and the main control algorithm 300.

However, if there has been a failure of the non-volatile RAM 16, then step 92 will direct the routine to the initialization step 94, as previously described, so that the set point and reference values lost from RAM 16 can be reinitialized by the values stored in PROM 18. In this manner, the above described invention detects and takes appropriate action in response to failures of the non-volatile RAM 16. This same invention also eliminates the need for time-consuming iterative redetermination of the set point and reference values based on the initialization values stored in PROM 18.

The conversion of the above-described flow chart into a standard language for implementing the algorithm described by the flow chart in a digital data processor, such as a microprocessor, will be evident to those with ordinary skill in the art.

While the invention has been described in conjunction with a specific embodiment, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the foregoing description. Accordingly, this invention is intended to embrace all such alternatives, modifications, and variations which fall within the spirit and scope of the appended claims.
The claims defining the invention are as follows:

1. In a control system having parameter sensing means, first storage means for storing a first data set, including a flag value, second storage means for storing a second data set and a stored program digital computer for generating control signals as a function of variables derived from the sensed parameters and the data sets by execution of a control algorithm, a memory failure detection system comprising:
   means for examining the status of the flag value stored in the first storage means;
   means for setting selected ones of the variables to values corresponding to the second data set prior to execution of the control algorithm when the flag value is in a first state, and for preventing setting of the selected variables to values corresponding to the second data set when the flag value is in a second state; and
   means for setting the flag value to its second state after the selected variables are set to the values corresponding to the second data set.

2. The invention of claim 1, wherein:
   the first storage means comprises a non-volatile random access memory (RAM);
   the second storage means comprises a programmable, read-only memory (PROM); and,
   the stored program digital computer comprises a microprocessor.

3. The invention of claim 2, wherein:
   the RAM has a dedicated power supply comprised of a battery coupled only to the RAM.

4. A control system substantially as herein described with reference to and as illustrated in the accompanying drawings.

DATED this 22nd day of December, 1983

DEERE & COMPANY
By their Patent Attorneys
ARTHUR S. CAVE & CO.
FIG. 1
START

IS BATTERY = 10101010?

NO

INITIALIZATION

YES

LOOP START

READ SENSED PARAMETERS

CALCULATE CONTROL SIGNAL

FIG. 2